REMARKS

Claims 1-23 are pending in the present application. Claims 1-5 are currently being considered, and Claim 1 is the sole independent claim currently being considered. Claims 6-23 have been withdrawn from consideration. Claims 1-3 and 5 have been amended. The Applicant has carefully and thoughtfully considered the Office Action and the comments therein. For the reasons given below, it is submitted that this application is in condition for allowance.

Rejections under 35 U.S.C. § 101

On page 1 of the Office Action, claims 1- 5 are rejected under 35 U.S.C. § 101 as allegedly being directed to non-statutory subject matter. Applicants respectfully disagree with the Office Action. Nonetheless, to further prosecution, claim 1 has been amended to more clearly recite the invention. Applicants therefore respectfully request that this rejection be withdrawn.

Rejections under 35 U.S.C. § 112

On page 3 of the Office Action, claims 1-3 and 5 are rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. Applicants respectfully disagree with the Office Action. Nonetheless, to further prosecution, claims 1-3 and 5 have been amended to more clearly recite the invention. Applicants therefore respectfully request that this rejection be withdrawn.

Rejections under 35 USC § 102

In the Office Action on pages 3-4, claim 1 is alleged to be anticipated by DAVID A. PATTERSON & JOHN L. HENNESSY, COMPUTER ARCHITECTURE A QUANTITATIVE APPROACH (2nd ed. 1996) (hereinafter Hennessy). Applicants respectfully disagree with this assertion.

The Office Action asserts that Hennessy discloses the elements of the method of amended claim 1. Amended claim 1 recites, "[a]n apparatus for data transfer, comprising: a direct memory access register to hold a descriptor, said register comprising: a command register comprising a single compare enable bit and a single branch enable bit; a source address register; a target address register; and a descriptor address register." Hennessy, however, does not teach or suggest all of the elements of claim 1, as will be shown, for at least the following two reasons.

First, Hennessy does not teach "a command register comprising **a single compare enable bit**." The Office Action's alignment of Hennessy with claim 1 is difficult to follow. To Applicant's best understanding, the Office Action is aligning the "branch condition" ("equal to zero" and "not equal to zero" in Figure 2.24) with the single compare enable bit of claim 1. Instead of teaching a single compare enable bit, Hennessy teaches a conditional branch operation. Hennessy, page 102. **In order to enable a branch operation, a condition must be satisfied**. Hennessy, page 102. The condition is specified by the instruction ('BEQZ' and 'BNEZ' in Figure 2.24). Hennessy, page 102. These instructions may examine a register ('R4' in Figure 2.24), having **32 bits**, to determine if the **value is equal to zero or nonzero**. Hennessy, pages 101-102. If the condition is satisfied, a branch operation will be performed. The branch address is specified with a 16-bit signed offset ('name' in Figure 2.24) that is added to the program counter. Hennessy, page 102. In contrast, the compare enable bit of claim 1 is recited as a **single bit**, whereas Hennessey teaches using a **conditional statement**. **Hennessy, therefore, does not teach "a single compare enable bit" as recited in claim 1.**

Second, Hennessy does not teach "a command register comprising a single compare enable bit **and a single branch enable bit**." The Office Action's alignment of Hennessy with claim 1 is difficult to follow. To Applicant's best understanding, the Office Action is aligning a register source value of zero or nonzero with the single branch enable bit of claim 1. Instead of teaching a single branch enable bit, Hennessy teaches a conditional branch operation. Hennessy, page 102. **In order to enable a branch operation, a condition must be satisfied**. Hennessy, page 102. The condition is specified by the instruction ('BEQZ' and 'BNEZ' in Figure 2.24). Hennessy, page 102. These instructions may test a register ('R4' in Figure 2.24), having **32 bits**, for a **value**

equal to zero or nonzero. Hennessy, pages 101-102. If the condition is satisfied, a branch operation will be performed. In contrast, the branch enable bit of claim 1 is recited as a **single** bit, whereas Hennessy teaches using **32** bits. **Hennessy, therefore, does not teach "a single branch enable bit" as recited in claim 1.**

Thus, applicants respectfully request withdrawal and reconsideration of the rejection of claim 1 under 35 U.S.C. § 102(b) as being anticipated by Hennessy.

Rejections under 35 USC § 103

In the Office Action on pages 5-7, claims 2-5 are rejected as being unpatentable over DAVID A. PATTERSON & JOHN L. HENNESSY, COMPUTER ARCHITECTURE A QUANTITATIVE APPROACH (2nd ed. 1996) (hereinafter Hennessy) in view of U.S. Patent No. 6,457,073 to Barry *et al.* (hereinafter Barry). Applicants respectfully traverse the rejection.

Dependent claims 2-5 are allowable, at least, for being dependent from an allowable claim.

Thus, applicants respectfully request withdrawal and reconsideration of the rejection of claims 2-5 under 35 U.S.C. § 103(a) as being anticipated by Hennessy in view of Barry.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is hereby invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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